The High Capacity and High Speed diffCDMA with the BCH Double Error Correction and Continuous Phase Primary Modulation

BCHダブル符合訂正機能と連続位相一次変調を用いた大容量高速 diffCDMA

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Abstract *It is shown in this paper that diffCDMA have high capacity with two degrees phase continuous primary modulating PSK and shortened BCH (62,50) ECC code for double error correction property. The diffCDMA improves transmission characteristics and robustness through such urban environment as rapid multi-ray Rayleigh fading channel in such similar CDMA systems as IS95 and the third generation IMT2000 system, when communications are carried from more then 100 mile/h running mobiles or 200 mile/h valet train.*

BCH error correction is also proposed here to give novel decoding method with finite group transformation, which is rather convenient from the existing Peterson's BCH decoding method.

1. INTRODUCTION

Typical IMT2000 CDMA is desired to communicate up to 2 Mbps with using less than 8 Mchip rate through 5 MHz bandwidth channel. The phase continuous primary DQPSK [1], which has proposed in VTC98 as the first solution for 2Mbps / 8 Mcps diffCDMA, is retrieved here to realize the more high reliability and high frequency efficiency 2 Mbps / 4 Mcps diffCDMA. Continuous phase primary modulation, is enhanced to newly proposing 2 Mbps / 4 Mcps diffCDMA with vanishing the catastrophic jump between successive adjacent symbols at around every period fringes.

In the demodulation procedure of the diffCDMA, receiving waves are at first detected after multi-ray propagation with certain inevitable errors both in phase and frequency of the receiving carrier as the pseudo synchronization primary demodulation. This pseudo synchronization primary demodulation produces instantaneous in- or quadrature- channel signal, after multiplying by arbitrary approximately recovered i- or q-channel carrier, respectively. Walsh function is employed for the direct spectrum spreading.

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The syndrome S^ of the diffCDMA employing shortened (62,50) BCH code, are defined by

$$\hat{S} = y * \hat{H} = S_1 + S_2 \qquad (1)$$

Where y is the receiving code word, S_1 and S_2 is partial syndromes of each row vector of size 12 bits, which are new notation for the error location of the first and the second errors. $\hat{H}$ is, therefore, also newly defined check matrix through group transformation of 62 rows and 12 columns matrix. position of the double errors is interpreted as the cyclic shift number of matrix **H**.

2. THE SYSTEM CONFIGURATION OF DIFFCDMA

2.1 Transmission Module Scheme

The transmission module of the diffCDMA with both phase continuity and shortened BCH (62, 50) ECC is shown in fig.1. The circuitry skeleton is almost the same to the existing CDMA transmission module only with exception of the two points. The former is employing the shortened BCH ECC circuit is pre-fixed to the input terminal. The later is phase continuity circuit CP, which is interpolated between differential code circuit DC and the primary modulator MOD for every transmission channel.

In fig.1, mark BI, BE, or SP means the binary information resource, encode of BCH code, or serial-to-parallel converter circuit, respectively. And, mark DC,CP, MOD, or DS/SS means the differential code, phase continuity circuit, the primary modulation, or the direct sequence/spread spectrum. Also mark WAL, P/MOD, or BPF/TX means Walsh spread spectrum code generator, pilot / modulation, or band-pass filter / Transmission unit, respectively.

The total number of diffCDMA transmission channel is 32 channels, where from 1 channel to 31 channels are devoted to carry information with BCH coding.

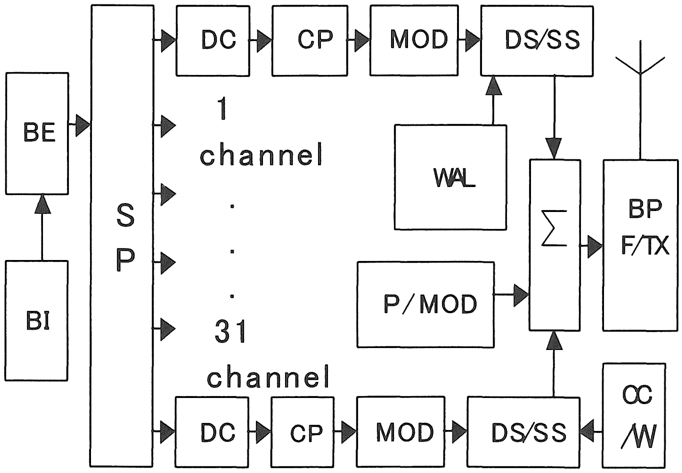

Fig.1 Block diagram of diffCDMA transmission module with phase continuous PSK and (62,50) BCH ECC

2.2 Receiving Module Scheme

As shown in fig.2, the circuit topology of the receiving module of the diffCDMA is also the same to the receiving module of the existing CDMA. Mark RX, deMOD, SYN, or CNT means the receiving unit, the primary demodulator, synchronization detector, or the control signal recovery circuit.

And, mark deSS, VSI, DEL, or DIF means the direct sequence spectrum de-spreading circuit, the virtual segment interleaving circuit, the delay time unit, or the differential decoding / decision circuit. The resting mark CG, P / de, PS, BD, BID means the spread spectrum de-code generator consists of Walsh function, pilot / demodulation, the parallel-to-serial converter circuit, the BCH decode unit, or the binary information destination, respectively.

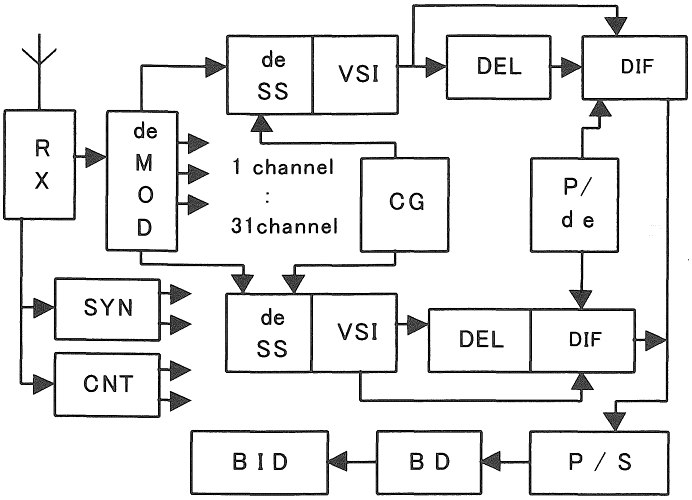

Fig.2 Block diagram of diffCDMA receiving module with phase continuous PSK and (62,50) BCH ECC

The total receiving channel number of diffCDMA is 32, from 1 channel to 31 channel are facilitated with BCH double error correction coding, the 0th channel is ordinal pilot channel without ECC. From the channel usage efficiency points of view, in the conventional CDMA, the transmission channel number m is required to be larger than receiving speech channel m', because of the control and synchronization signal are either carried through the redundant m-m' channels in both cdmaOne and cdma2000. Even if in the W-CDMA, the maximum transmission is carried by redundant time slot shared with time compression to yield equivalent redundancy both on time and frequency space. The previously reported diffCDMA, which implicitly employs pilot and control signals for every symbol over individual channel, has perfectly succeeded in excluding such redundancy of pilot and time slot.

Fortunately, the computer simulations are verified for the diffCDMA to be error free through such poor propagation as two-ray Rayleigh fading.

2.3 Signal Scheme of 2 Mbps of diffCDMA

Reducing CDMA bandwidth is important not only for high efficiency of frequency usage but also for preventing both from fading bandwidth expansion and spectrum distortion through multi-ray propagation environment. In the previously reported diffCDMA, employing the $\pi/4$ -DQPSK is employed as the primary modulation to reduce the frequency occupancy [2]. In this paper, the signal scheme of the diffCDMA every channel is shown in fig.3, SEG and VSI means fundamental segment and virtual segments, which are interleaving among these fundamental segments. In order to transmit 2 Mbps, the diffCDMA requires that every symbol duration is consist of 4 segments and 3 virtual segments, where all these segments are themselves consist of 32 chips. The chip rate is given by for diffCDMA as 32 Ksymbol/sec × 4 seg./frame × 32 chip/seg. = 4.094 Mcps.

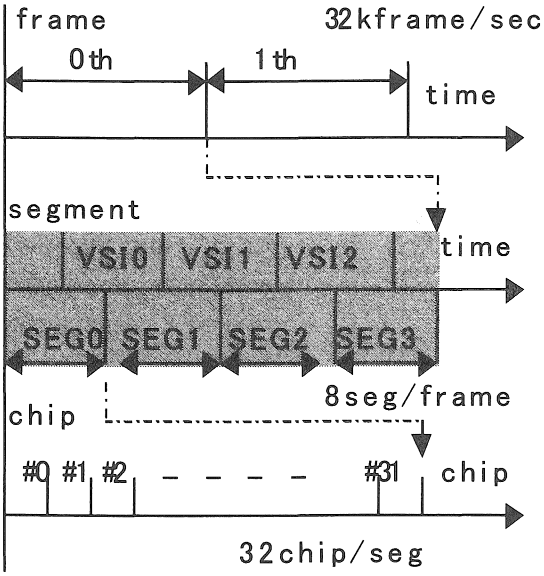

Fig.3 Signal scheme in 2Mbps diffCDMA

3. DOUBLE ERROR CORRECTION

3.1 Group Transmission Check Matrix, *H*

The BCH error correction codes are well known well in keenly studying by Hocquenghem, Bose and Chaudhuri in 1959 and 1960 [3]. For the diffCDMA, we try to adopt (62, 50) BCH double error correcting code, the algebraic structure of BCH code is defined by the generating polynomial G(x). Because of the four minimal polynomials, $M_1(x)$, $M_2(x)$, $M_3(x)$, and $M_4(x)$, have roots of the same minimal polynomial of a field element in $GF(2^6)$, therefore the generating polynomial G(x) of double error correction BCH code is defined and rewrite as [4],

$$G(x) = LCM\{M_1(x), M_2(x), M_3(x), M_4(x)\}$$

$$= LCM\{M_1(x), M_3(x)\}$$

$$= (x^6 + x + 1) *$$

$$(x^6 + x^4 + x^2 + x + 1) \qquad (2)$$

Here, LCM stands for least common multiples, $M_1(x)$ and $M_3(x)$ are degree 6 minimal polynomials.

According to generator polynomial G(x) functions, we get the 63 rows and 12 columns parity-check matrix, which is also called by check matrix **H**, without any shortened information. In general speaking, the conventional check matrix **H** is given as shown in the followings, and rewritten after modulus (α^i, α^{63}) operations. Here, α is a primitive element of $GF(2^6)$.

$$\mathbf{H} = \begin{vmatrix} \alpha^{62}, \alpha^{61}, \ldots\ldots \alpha^{4}, \alpha^{3}, \alpha^{2}, \alpha^{1}, \alpha^{0} \\ \cdot \quad \cdot \quad \ldots\ldots \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \\ \alpha^{186}, \alpha^{183} \ldots\ldots \alpha^{12}, \alpha^{9}, \alpha^{6}, \alpha^{3}, \alpha^{0} \end{vmatrix}^{T}$$

$$= \begin{vmatrix} \alpha^{62}, \alpha^{61}, \ldots\ldots \alpha^{4}, \alpha^{3}, \alpha^{2}, \alpha^{1}, \alpha^{0} \\ \cdot \quad \cdot \quad \ldots\ldots \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \\ \alpha^{60}, \alpha^{57} \ldots\ldots \alpha^{9}, \alpha^{9}, \alpha^{6}, \alpha^{3}, \alpha^{0} \end{vmatrix}^{T} \qquad (3)$$

The conventional check matrix **H** through finite group transform being become reduced echelon form **H^**, expressed linear combinations of the information as systematic code form. The finite group transmission matrix holds both cyclic [5] and mirror formulations. When the code word is shortened by one bit, **H^** is modified from 63 × 12 matrix to 62 × 12 matrix as follows.

$$\hat{\mathbf{H}} = \begin{vmatrix} \alpha^{28}, \alpha^{48}, \ldots\ldots \alpha^{4}, \alpha^{3}, \alpha^{2}, \alpha^{1}, \alpha^{0} \\ \cdot \quad \cdot \quad \ldots\ldots \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \\ \alpha^{51}, \alpha^{10}, \ldots\ldots 0, \quad 0, \quad 0, \quad 0, \quad 0 \end{vmatrix}^{T}$$

$$= [\mathbf{P}, \ \mathbf{I}_{12}]^{T} \qquad (4)$$

*Here, **P** is a parity matrix of 50 rows by 12 columns,* $\mathbf{I}_{12}$ *is systematic 12 dimensional identity matrix for double error correction.*

The new check matrix **H^** given by *reduced echelon form* for double error detecting and correction expresses two properties, combinatory linearity and cyclic shift that will be reported in the near future. The first combinatory linearity is not only applied in double error correcting but also applied in t-error correction, here t>2. When t-error occur in transmit channel, the syndrome S^ are also defined by following equation, through group transmission.

$$\hat{\mathbf{S}} = \sum_{j=1}^{t} \mathbf{e}_j * \hat{\mathbf{H}} == \sum_{j=1}^{t} \mathbf{S}_j \qquad (5)$$

Here, $\mathbf{e}_j$ *is error vector,*

$\hat{\mathbf{H}}_j$ *is* 62×12 *matrix.*

This metrology is successfully verified through computer simulations both in detecting and correcting errors in (63,36) up to t=5 BCH ECC.

3.2 Soft Decoding Algorithm for BCH ECC

The soft decoding method for BCH error correction is new and different method from previously reported methods, iterative algorithm by Berlekamp, a related algorithm by Massey, and the search algorithm by Chien and etc.

Let us consider an arbitrary code x to be transmit though the diffCDMA. The received code, y is written by,

$$\mathbf{y} = \mathbf{x} + \mathbf{e}_l + \mathbf{e}_j, \qquad (6)$$

Here, $\mathbf{e}_l$ *and* $\mathbf{e}_j = (e_1, e_2, e_3, \cdots, e_{62})$ *denote error vectors.*

If no errors occur in the first and j-th word positions, the syndrome is defined in corresponding to the receiving word **y** as S^ $= \mathbf{y} * \mathbf{H}^\wedge = (\mathbf{x} + \mathbf{0} + \mathbf{0}) * \mathbf{H}^\wedge = \mathbf{0}$, where **0** is the all-zero row vector of size 12. When both the first error and the second error occur in the in the 1st and j-th positions, since

$$S^\wedge = \mathbf{y} * \mathbf{H}^\wedge = (\mathbf{x} + \mathbf{e}_l + \mathbf{e}_j) * \mathbf{H}^\wedge \qquad (7)$$
$$= \mathbf{0} + \mathbf{e}_l * \mathbf{H}^\wedge + \mathbf{e}_j * \mathbf{H}^\wedge$$
$$= S_1 + S_2 \mid \mathrm{mod}2$$

The syndrome S^ is the same to the existing syndrome S. Unfortunately, S does not identify the error location uniquely.

However, the S_1 and S_2 of the new portion syndrome S^, which is new notation about error location of the first error and the second error, are able to uniquely identify the each location of the double errors. The relation between S_1 and S_2 values is discussed in the followings to formulate the one row vector value of **H^**.

The S_1 value is equal in magnitude meanings to the 1st row vector of **H^**, and the magnitude of S_2 is also uniquely equal to the j-th row vector of **H^**.

The new soft decoding method with bases on the relation that the inverts of the 1st or j-th row value of **H^** is equal in error locations to the summations for each syndrome for the receiving double errors. The new decoding method does not rely on such Newton's identities, error location polynomial, and etc. The double error decoding for BCH error correction code is became to be simple as follows.

Implementation is easily performed by merely comparing S_1 and S_2 values with vector value of **H^** after cyclic shifting, if S_1 and S_2 equal to vector value. The error is, therefore, detected in its a priori position as the value through direction of the cyclic shifting number of **H^**.

The first error and the second errors are assumed for a example to be encountered in 19th and 48th in code word positions. That is,

S_1: 001111100110⇔18th row vector of **H^**

S_2: 000111011101⇔48th row vector of **H^**

S : 001000111011

3.3 Hard Circuit for Decoding and Computer Simulation Results

Employing the relation between syndrome and the H^, the new hard

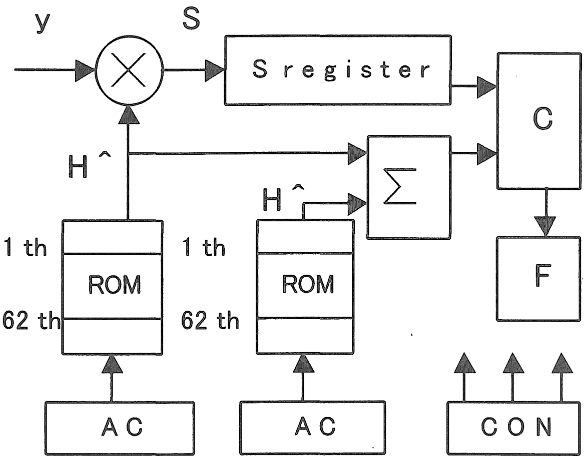

Fig.4 Function block diagram of the BCH decoder

decoding circuit is easily realized as shown in fig.4, in which the mark F, C, or SREG means the flag bit, the comparator of size 12 di-bits, or syndrome register of size 12 bits, respectively. And mark ROM and AC mean read only memory and addressing counter for ROM, all vector of **H**^ are stored into ROM. Mark CON means control circuit to control all these elements.

When double errors occur in arbitrary positions, then the value of syndrome register is not equal zero, compare the value of syndrome with summation of double ROM value until the flag bit circuit equal 1, when the double address counters become to show the double error occurrence in error positions.

The computer simulations are verified that proposing BCH ECC shows the sufficient effect in error correcting to put 1.6 Mbps/4Mcps diffCDMA on developing stages through such poor radio channel as two-ray Rayleigh urban environments of 0.5 micro second delay spread from bullet trains.

BER vs. CNR is shown in the Fig.5, the horizontal axis means carrier to noise ratio, CNR, vertical means BER, with taking status of without error correction, single error correction, or double error correction as parameters.

Pay attentions on that CNR is employed in these simulations instead of Eb/No, because plural 32 codes are devoted to carry 1.6 Mbps through whole 32 channels of 32k symbol rate in the Walsh function of length 32. Error free is observed for 1.6Mbps/ 4Mcps diffCDMA from 300km/h running bullet train at around CNR=12dB as BCH double error correction. This simultaneously means error free around at Eb/No=-6dB after compensation of 10log64.

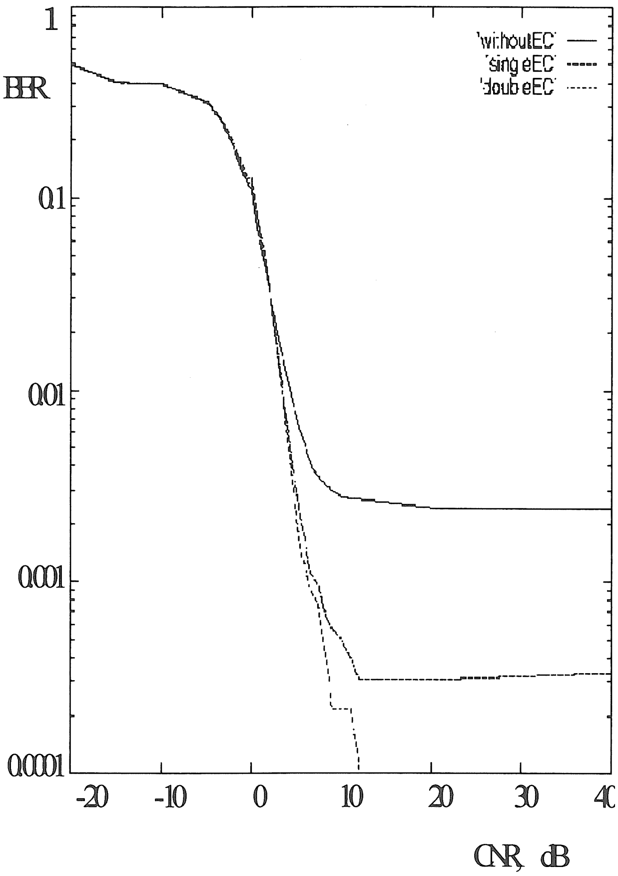

Fig.5 BER vs. CNR response comparison among bullet train communications with single error correction, double error correction, and without error correction of 1.6 Mbps/ 4.096MHz diffCDMA through two ray Rayleigh environment with 0.5 micro second delay spread

4. CONCLUTION

The diffCDMA is successfully verified to be error free over 1.6Mbps / 4Mcps with employing both BCH ECC (62,50) and phase continuous primary modulation through such computer simulations as following conditions. The carrier frequency is on 2GHz domain, Walsh function length is 32, symbol rate is 32 k symbol / sec, the fundamental segment number of the Walsh is 4, i.e. 7 virtual segments are employed for every symbol. The fdT is 0.015, doppler shift is 0.3ppm, and the occupied transmission bandwidth is 4MHz. The frequency usage efficiency is observed to be 0.4 bit/Hz, and BER to be zero beyond CNR= 12dB.

The diffCDMA is verified to transmit through such urban propagation circumstance as two-ray Rayleigh fading of DUR= 10dB with 0.5 micro second delay spread from 300km/h running bullet trains.

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(受付 平成１２年３月１８日)